I CLAIM:

1 A CMOS integrated circuit device comprising:

a plurality of p-channel transistors formed in active surface areas of n-type regions;

a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;

gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and being insulated from the respective active surface areas;

p-type source and drain regions for the p-channel transistors, each p-type source and drain region consisting of a low resistivity region;

n-type source and drain regions for the n-channel transistors, each n-type source and drain region having a low resistivity region and an LDD region;

each gate electrode having a pair of sidewall spacers each having an inner and an outer portion, each sidewall spacer corresponding to an underlying source and drain region;

each p-channel low resistivity region located under the outer portion and at least a part of the inner portion of its respective sidewall spacer;

each n-channel low resistivity region located under at least a part of the outer portion and a part of the inner portion of its respective sidewall spacer; and

each n-channel LDD region extending from its respective low resistivity region to underlie the inner portion of its respective sidewall spacer.

2 The integrated circuit of claim 1, wherein the inner portion of the sidewall spacer comprises an oxide.

3 The integrated circuit of claim 1, wherein the outer portion of the sidewall spacer comprises an oxide.

4 The integrated circuit of claim 1, wherein the p-channel source and drain comprise silicon implanted with BF_2.

5 The integrated circuit of claim 1, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the transistor will not operate reliably due to short channel effects; and,

the p-channel maximum length is a distance the above which the transistor will not turn on efficiently.

6 The integrated circuit of claim 1, wherein the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor will not turn on efficiently.

7 The integrated circuit of claim 1, wherein the sidewall spacers have a total width of approximately 500 to 2500 Å.

8 A method of fabricating p-channel and n-channel transistors in a CMOS device, the method comprising:

forming gate electrodes for p-channel and n-channel transistors over n-type and p-type silicon regions that define isolated active areas of the device;

implanting an n-type dopant into the p-type silicon region to form LDD regions of the n-channel transistor;

forming a first insulating layer over the gate electrodes and the n-type and p-type silicon regions;

implanting a p+ type dopant into the n-type silicon region for forming low resistivity source and drain regions of the p-channel transistor;

forming a second insulating layer over the first insulating layer;

etching the first and second insulating layer to provide sidewall spacers over the silicon regions adjacent to the gate electrodes; and

implanting an n+ type dopant impurity into the portions of the p-region for forming low resistivity portions of source and drain regions of the n-channel transistor.

9 The method of claim 8, further comprising the step of diffusing the p+ type implant toward the respective gate, performed after the step of implanting the p+ type dopant.

10 The method of claim 8, further comprising the steps of:

masking the n-type silicon regions, performed prior to the step of implanting the n-type dopant to form the LDD regions, for masking the n-type silicon regions from the n-type dopant implantation; and

unmasking the n-type silicon regions, performed after the step of

implanting the n-type dopant;

masking the p-type silicon regions, performed prior to the step of implanting the p+ type dopant, for masking the p-type silicon regions from the p+ type dopant implantation;

unmasking the p-type silicon regions, performed after the step of implanting the p+ dopant and before the step of forming a second insulating layer;

masking the n-type silicon regions, performed prior to the step of implanting the n+ type dopant, for masking the n-type silicon regions from the n+ type dopant implantation; and

unmasking the n-type silicon regions, performed after the step of implanting the n+ dopant.

11 The method of claim 8, wherein the first insulating layer comprises an oxide.

12 The method of claim 8, wherein the second insulating layer comprises an oxide.

13 The method of claim 8, wherein the p+ type dopant impurity comprises BF_2.

14 The method of claim 8, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the

transistor will not operate reliably due to short channel effects; and

the p-channel maximum length is a distance above which the transistor will not turn on efficiently.

15 The method of claim 8, wherein the first insulating layer has a thickness of approximately 500 to 2500 Å.

16 The method of claim 8, wherein the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor will not turn on efficiently.

17 The method of claim 8, wherein the second insulating layer has a thickness of approximately 500 to 2500 Å.

18 The method of claim 8, wherein the sidewall spacer comprises an inner portion, formed from the first insulating layer, and an outer portion, formed from the second insulating layer.

19 A method of fabricating p-channel and n-channel transistors, the method comprising:

forming gate electrodes for p-channel and n-channel transistors over n-type and p-type silicon regions, the gate electrodes being separated by a region of isolation insulating;

masking the n-type silicon region;

implanting an n-type dopant into the p-type silicon region to form LDD and halo implants;

unmasking the n-type silicon region;

forming a first insulating layer over the gate electrodes and the n-type and p-type silicon region;

masking the p-type silicon region;

implanting a p+ type dopant into the n-type silicon region for forming source and drain regions of the p-channel transistor;

unmasking the p-type silicon region;

forming a second insulating layer over the first insulating layer;

etching the first and second insulating layer to provide sidewall spacers over the silicon regions adjacent to the gate electrodes;

masking the n-type silicon regions;

implanting an n+ type dopant into the p-type silicon regions for forming low resistivity regions of source and drain regions of the n-channel transistor;

unmasking the n-type silicon regions;

diffusing the p+ type implant toward the gate electrode.

20 The method of claim 19, wherein the first and second insulating layer

comprise oxide.

21 The method of claim 19, wherein the p+ type dopant impurity comprises BF_2.

22 The method of claim 19, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the transistor will not operate reliably due to short channel effects; and

the p-channel maximum length is a distance above which the transistor does not turn on efficiently.

23 The method of claim 19, wherein the first insulating layer has a thickness of approximately 500 to 2500 Å

24 The method of claim 19, wherein the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor does not turn on efficiently.

25 The method of claim 19, wherein the second insulating layer has a

thickness of approximately 500 to 2500 Å.

26 The method of claim 19, wherein the sidewall spacer comprises an inner portion, formed from the first insulating layer, and an outer portion, formed from the second insulating layer.